

Appl. No. 10/694,592
Amdt. Dated July 28, 2008
Reply to Office Action of February 28, 2008

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SPECIFICATION AMENDMENTS

Page 5, lines 10-31, replace the paragraph with:

In order to assist understanding of the potentials that occur on the bus lines 7, 8 during data transmission, ~~Figure 1b~~ Fig. 1B uses one of the transceivers 2a to illustrate, schematically, the internal configuration of the transceivers with the circuit components that are necessary for data transmission. The transceiver 2a has a voltage regulator 25, which produces a voltage VCC with respect to an internal reference ground potential GND2 in the transceiver 2a, in order to make a high potential VCC2 available in the transceiver. The reference ground potential GND2 in the transceiver 2a corresponds to the reference ground potential GND in the overall arrangement when no ground shift is present, and, in the case of a ground shift, is shifted through a value GND_{shift} with respect to the reference ground potential GND or ground. When there is no ground shift in the transceiver, the high potential VCC2 then corresponds to the potential VCC and, when a ground shift is present, it corresponds to the value $VCC + GND_{shift}$. A low potential which is available in the transceiver corresponds to the internal reference ground potential GND2.

Page 7, lines 4-11, replace the paragraph with:

~~Figure 2a~~ Fig. 2A shows the profile of the two potentials VCANH, VCANL on the CANH line 7 and on the CANL line 8 for ideal, interference-free operation,

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when no ground shift is present, that is to say when $VCC2=VCC$ and $GND2=GND$, with VCC denoting the voltage VCC which is available in all of the transceivers 2a-5a, and with GND denoting the low potential which is available in all of the transceivers 2a-5a.

Page 8, lines 6-18, replace the paragraph with:

~~Figure 2b~~ Fig. 2B shows a fault situation in a system in which there is no ground shift, in which situation the CANL line has a short circuit to this supply voltage V_{bat} , with this voltage being greater than the high potential VCC . In order to detect a short circuit such as this from one of the bus lines 7, 8 to the supply potential V_{bat} , it is known for the potentials on the bus lines 7, 8 in at least one of the transceivers to be compared by means of a comparator, which is not illustrated in any more detail, with a threshold voltage which is higher than the high potential VCC , and for a fault to be output if the potential on one of the bus lines 7, 8 exceeds this comparator threshold.

Page 14, lines 31-37, replace the paragraph with:

In order to describe the method according to the invention, the bus system in which the method according to the invention is used will be described in more detail first of all. This bus system may, for example, have the configuration illustrated in ~~Figure 1~~ Fig. 1A, although other refinements of the bus system are also feasible.

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Page 15, lines 1-7, replace the paragraph with:

In the block diagram shown in ~~Figure 1~~ Fig. 1A, the reference symbol 1 denotes the bus system according to the invention. The following text is based on the assumption that the networked bus system is a CAN bus system, in particular a so-called low-speed CAN bus system, although the invention is not restricted to this.

Page 15, lines 9-21, replace the paragraph with:

In the manner which has already been explained, the bus system in ~~Figure 1~~ Fig. 1A has four bus subscribers 2 - 5, which are also referred to as modules or communication stations. For serial transmission of binary data by means of duplex signals, these bus subscribers 2 - 5 are coupled to a differential two-wire, typically twisted, data bus 6, with the data communication between the bus subscribers 2 - 5 which are connected to the bus 6 taking place in a known manner, which has already been explained in the introduction. The reference symbol 7 denotes the CANH line, and the reference symbol 8 denotes the CANL line of the data bus 6.

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Page 15, lines 23-38, replace the paragraph with:

The physical coupling to the two-wire bus 6 is carried out via the transmitting and receiving device 2a - 5a, the so-called transceiver, which is contained in each bus subscriber 2 - 5 and is designed for transmitting and/or receiving data via the data bus. For data transmission, the transmitting and receiving devices 2a - 5a convert the data to be transmitted in the explained manner, with this data being provided by the respective control unit 2b-5b, from a logic level within the relevant bus subscriber 2-5 to two complementary transmission signals, whose waveform for normal interference-free operation is illustrated in ~~Figure 1~~ Fig. 2A. For data reception, these transmission levels are converted by the transceivers 2a-5a to logic signals, which are processed further by the control units.

Page 16, lines 17-34, replace the paragraph with:

The individual bus subscribers have an internal high potential and an internal low potential in order to ensure the data transmission as explained initially. As already explained, it is possible for the individual bus subscribers 2 - 5 to have an offset in their reference ground potential, the so-called ground shift. Only the bus subscriber 2 has such a ground shift in ~~Figure 1~~ Fig. 1A. This ground shift potential GND_{shift} ensures that the internal low potential $GND2$ of this subscriber is higher than the reference ground potential GND by the value GND_{shift} . Although only the bus subscriber 2 has a ground shift in Figure 1, this

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effect may, of course, also occur in the other bus subscribers 3 - 5, and possibly to a different extent. The design of such a bus subscriber 2 with ground shift in general and of the corresponding transceiver 2a in particular will be described in more detail in the following text with reference to Figure 3.

Page 16, line 36 through page 17, line 9, replace the paragraph with:

The internal high potential VCC2 can be applied to the CANH line 7, and the internal low potential GND2 can be applied to the CANL line 8 via the switching devices S21, S22 which are illustrated in ~~Figure 1b~~ Fig. 1B for the subscriber 2 and which, correspondingly, are also provided in one or more of the other bus subscribers 3 - 5. If there is no ground shift in the system, the internal high potential in all of the subscribers 2-5 corresponds to the value VCC, and the internal low potential in all of the subscribers 2-5 corresponds to the reference ground potential GND, with VCC denoting a voltage which is provided by an internal voltage regulator.

Page 18 lines 1-2, replace the paragraph with:

~~Figure 3~~ Fig. 3 shows a block diagram of the configuration of a bus subscriber which has a ground shift.

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Page 18, lines 14-38, replace the paragraph with:

The bus subscriber 2 which is illustrated in ~~Figure 1~~ Fig. 3 also has an evaluation circuit 20, whose input side is connected to the lines 7, 8. The evaluation circuit 20 is in this case a component of the transceiver 2a. The evaluation circuit 20 has first to fifth comparators 21 - 25 as data detection means or fault detection means, with the first, second and fourth comparators 21, 22 and 24 being connected on the input side to the CANH data line 7, and the first, third and fifth comparators 21, 23, 25 being connected to the CANL data line 8. The first comparator 21 in this case forms the differential input of the transceiver, and compares the signals VCANH, VCANL on the data lines 7, 8, while the second and fourth comparators 22, 24 compare the signal VCANH on the data line 7 with a first and second reference potential Vref1, Vref2, respectively, and the third and fifth comparators 23, 25 compare the signal VCANL on the data line 8 with a third and a fourth reference potential Vref3, Vref4, respectively. The first to fourth reference potentials Vref1-Vref4 are each related to a reference ground potential or low potential GND2 of the evaluation circuit, with this reference ground potential GND2 in the example having a ground shift GND_{shift} with respect to the ground potential GND.

Page 19, line 37 through page 20, line 6, replace the paragraph with:

If a fault now occurs, in which the CANH line 7 is permanently at a supply potential Vbat, as is illustrated in ~~Figure 2b~~ Fig. 2B, then the output signal from

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the comparator 21 assumes a high level permanently, provided that, taking into account the ground shift, this potential V_{bat} is greater than $VCC2 = VCC + GND_{shift}$. It is thus no longer possible to reconstruct the data transmitted via the bus from the output signal 31 from the first comparator 21.

Page 22, lines 6-23, replace the paragraph with:

In this state, the CANH line 7 is connected via a switching device (which is not illustrated in any more detail in ~~Figure 3~~ Fig. 3) to a high potential which corresponds approximately to the potential $VCC2$. This potential $VCC2$ is produced in the manner that has been explained by means of a voltage regulator, which is not illustrated in any more detail but which produces a voltage VCC related to the internal low potential $GND2$, which is higher at GND_{shift} than the ground potential GND . The comparison voltage V_{ref1} from the first comparator is higher than the voltage VCC , so that the threshold $V_{ref1} + GND_{shift}$ of the CANL line 7 is never reached during defect-free operation. A fault is identified only when V_{CANH} becomes greater than $V_{CANH} + GND_{shift}$, for example as a result of a short circuit to a supply voltage which is greater than $VCC2$. The supposed detection of a short circuit on the CANH line 7 as a result of a ground shift is precluded.

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Page 23, lines 1-9, replace the paragraph with:

Figure Fig. 4 uses a block diagram to show one exemplary embodiment of the fault identification circuit 27, by means of which a short circuit between the CANH line 7 and a supply voltage and between the CANL line 8 and a supply voltage can be identified. To assist understanding, the illustration likewise shows the comparators 21, 22, 23 which produce the input signals for this device.

Page 26, lines 11-17, replace the paragraph with:

The circuit which is illustrated in Figure Fig. 4 thus produces fault signals for further processing only when the respective output stage is in the dominant mode. Furthermore, the evaluation circuit 20 is designed to detect line faults independently of the presence of any ground shift, and nevertheless to carry out data detection even when a line fault has been detected.

Page 26, lines 19-28, replace the paragraph with:

In principle, the same circuit as that in ~~Figures 1~~ Figs. 1A, 1B, 3 and 4 can be used for a high-speed CAN bus system in order to identify the corresponding faults. However, in this case, the delay times must be appropriately matched to the higher speed of the bus system. In this case, however, the fault ERR3, that is to say a short circuit between the line 7 and the supply voltage VCC, is less

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informative, since data transmission is no longer possible at all in this situation
owing to the high-speed bus configuration.